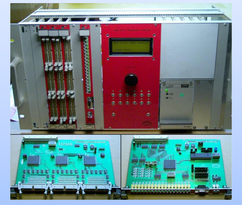
SERVIZIO ELETTRONICA E RIVELATORI

A. Anastasio, **A. Boiano**, A. Bove, A. Buscemi, C. Caiazzo, L. Caiazzo, A. Candela, A. Carola, A. Cascini, R. Chiaramonte, M. Cipriano, **P. Di Meo**, M. Di Pietro, **S. Energico**, A. Lauro, F. Manna, G. Manto, **V. Masone**, **A. Pandalone**, A. Parmentola, **L. Parascandolo**, P. Parascandolo, A. Perricone, R. Pesce, P. Salmas, C. Sogaro, C. Tornatore, **P. Trattino**, **A. Vanzanella**

ESPERIMENTO CMS

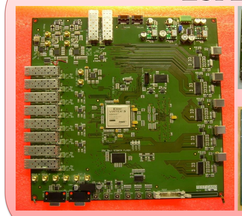
Link Board Upgrade

Control Board Upgrade



CMS Frequency Meter

ESPERIMENTO FAZIA



Block-Card
- Concentratore di dati tramite 16 link a 400Mbps
- Recupero e distribuzione dei segnali di clock a latenza fissa con jitter di 20ps (rms)
- Link ottico a 3Gbps

Test-card
- Concentratore di dati verso il PC di acquisizione
- Gestione dei trigger, del tempo assoluto e dell'event counter

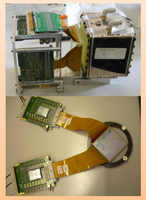
ESPERIMENTO JEM-EUSO

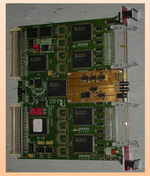
Clock Board

GPS Board

Data Processor System

ESPERIMENTO EXOTIC





TSV Board

- Gestione di un chip ASIC per la lettura di rivelatori al silicio (32 + 32 strips)
- 32 Canali d'ingresso di carica
- Proposte di trigger per singolo layer del rivelatore con soglie modificabili
- Sistema di acquisizione digitale su bus VME per la gestione in remoto di coincidenze fra 64 rivelatori

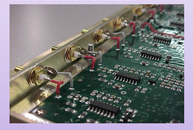
ESPERIMENTO Mu-RAY

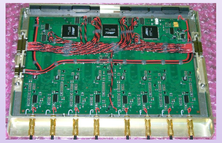
EASI Board
- Gestione completa delle funzionalità del chip EASIROC
- Sistema di alimentazione selezionabile tra Single o Multi Power
- Internal clock 250MHz
- Interfaccia USB
- Circuito di Time Expansion analogico
- Uscite High Gain e Low Gain acquisite mediante ADC a 12 bit

ESPERIMENTO PAMELA

DSP Board

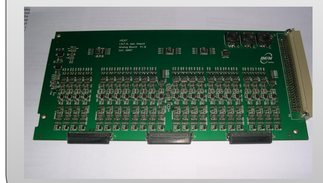
TOF Board Particular





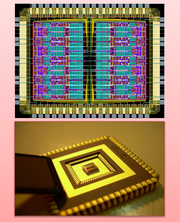
TOF Board

ESPERIMENTO AUGER



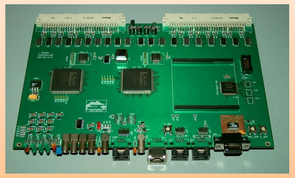
Analog Board
- Condizionamento di segnali analogici provenienti dai fotomoltiplicatori
- 22 canali d'ingresso
- Amplificatore a guadagno variabile
- Low Noise design (3.2 nV√Hz)

MAGMA CHIP



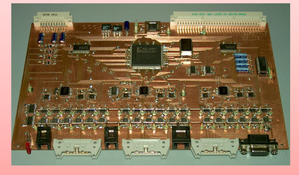
	FAST OUTPUT	SLOW OUTPUT
Peaking Time	300ns	2µs
Gain	5,7 mV/MeV	7,5 mV/MeV
Linearity	0,8%	0,18%
Resolution		13bit @20pF
Noise Slope		12eV/ pF
Dynamic Range	-180MeV ÷ +180MeV	
Input Channel	16	
Dissip. Power	~15 mW/Channel	

ESPERIMENTO OPERA



Controller Board
- Lettura e gestione di 9 Front-End Board
- Funzionalità di soppressione degli zero sui dati acquisiti
- Presenza di un modulo Linux Based per il trasferimento dei dati in standard Ethernet

ESPERIMENTO ICARUS



LTCU Board
- 18 ingressi analogici a soglie programmabili
- DAC a 8 bit controllabili via RS-232
- Uscite di Fast-Or e di Monitor
- Gestione via RS-232 o mediante protocollo dedicato

ESPERIMENTO ARGO

AMB Board

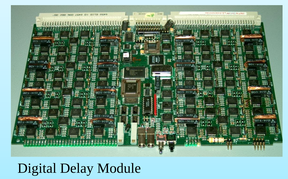
TRG Board

Power Supply

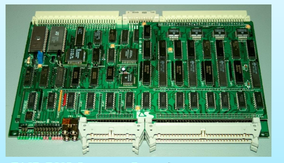
Majority Board

Charge Meter Board

ESPERIMENTO FAIR

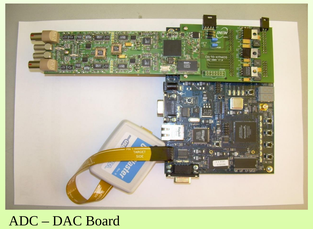


Digital Delay Module



FAIR BUS Segment Control

ESPERIMENTO VIRGO

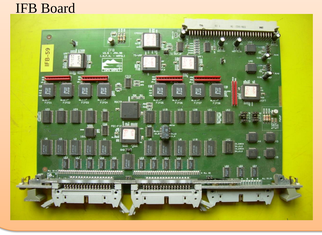


ADC – DAC Board

Dual channel module

ESPERIMENTO BaBar

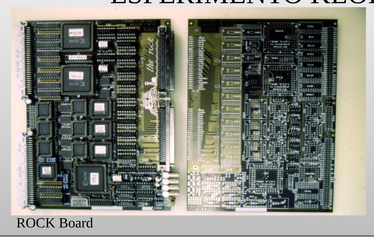
IFB Board



Positive FEC

Negative FEC

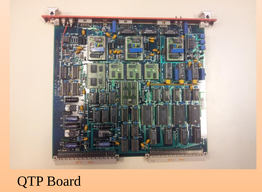
ESPERIMENTO KLOE



ROCK Board

AUXBUS

ESPERIMENTO MACRO

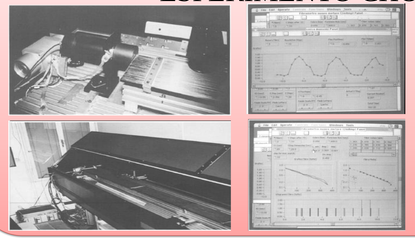


QTP Board

Readout Strip Board

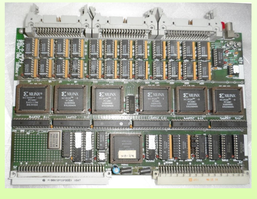
QTP Panel

ESPERIMENTO CHORUS



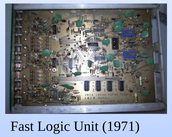
Il Fibrometro
L'apparato effettuava un controllo di qualità delle fibre scintillanti. Un sistema automatizzato permetteva di scartare le fibre fuori specifica in termini di emissione e attenuazione di luce.
Furono misurate 12000 fibre.

ESPERIMENTO L3



Zero Suppressor Board
- 96 ingressi provenienti dagli RPC
- Canali mascherabili singolarmente
- Pattern di test sui singoli ingressi
- Interfaccia su VME Bus in modalità memory mapped

ESPERIMENTO $B\ \bar{B}$



Fast Logic Unit (1971)

Fast Pulse Amplifier (1973)

16 Input Gated OR (1972)

ATTIVITA' CAD

- Suite di sviluppo ALTIUM DESIGNER
- Realizzazione di schede double-layer mediante Quick-Circuit Prototyping System